DESIGN OF SWITCHBOX ROUTER USING NEURAL NETWORK

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Abstract: In this paper, a new algorithm using maximum neural network for the topological via minimization problem in a switchbox is presented. The switchbox is the rectangular region allows its interconnection terminals on all four sides of the region. Maximum neural network with M-clusters for N-outputs is used to allocate M of two-terminal nets to N routing layers. This algorithm optimizes the terminal connectors into variable layers to minimize the number of via. This algorithm designed the digital hardware using VHDL, verified with Simulation tools and was fabricated by SK hynix 0.8μm CMOS process. The chip can solve the problem which contains the 10 terminal connectors and 2 layers.

Keywords - FPGA, Neural Network, Router, Switch box, VLSI.

I. INTRODUCTION

A problem of wiring between arranged chips or parts in the design stage of a printed circuit board (PCB), in particular, a problem of minimizing vias through optimized wiring has received much attention and attention. The via minimization problem is divided into several categories, the channel wiring problem and the switch box problem. In addition, in terms of prior information of lines to be relocated, there are CVM (Constrained Via Minimization) and TVM (Topological Via Minimization) problems to be addressed in this paper. In the case of the TVM problem, only the information on pins to be connected and the number of usable layers is determined, but the layers where other lines are located, the number of vias, and locations are not determined. In this TVM problem, minimizing the number of required vias by determining the phase of the connection lines is the ultimate goal of solving the problem. In this paper, neural network hardware capable of routing up to 10 connection lines with two layers of wiring was implemented as an ASIC [1-3].

II. PCB ROUTING PROBLEM

A. PCB Routing

PCB routing is the electrical connection according to the connection information after arranging the parts necessary to manufacture the designed circuit on the PCB, and Global Routing, which divides the area and places each connection line in a specific routing area, and divided areas It is divided into a Detailed Routing process that makes necessary connections by properly arranging the connection lines within each wiring layer. When dividing an area in Global Routing, it is divided into two areas: switch box and channel. In this paper, we are going to deal with Detailed Routing in the switch box [4,5].

B. Switch Box

A switch box is a rectangular area without any obstacles inside the routing area, and terminals can be located on all four sides and connections can be made in all directions. This is a generalized channel where terminals are located on two parallel sides and connections are made between the terminals on both sides. Figure 1 shows an example by dividing the lines arranged on layers 1 and 2 with solid and dotted lines.

Routing in the switch box has been developed many algorithms because of its importance in Detailed Routing. In this paper, this problem was solved by using the maximum neural network model [6,7].

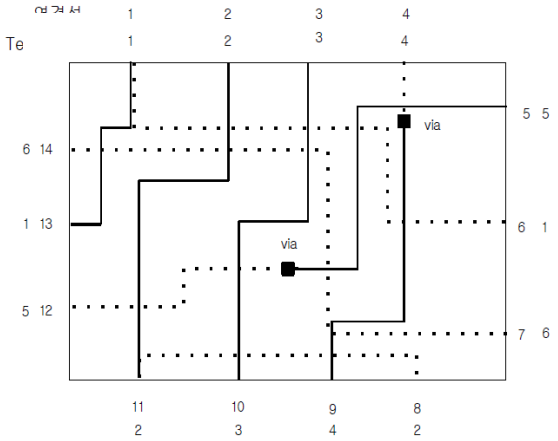


Figure. 1: Switch Box

III. MODELING A SWITCHBOX ROUTER USING NEURAL NETWORKS

A. Maximum Neural Network Model

The maximum neural network model is a neural network model that expresses the system as energy and obtains the desired solution by flowing along the surface of the energy function. The input and output of neurons are represented by U and V, respectively, and are composed of M clusters composed of N neurons. Among the N neurons belonging to each cluster, only the neuron with the highest sum of inputs Ui,j has an output of 1. and other neurons have an output of 0. Mathematically expressed, the

input/output function of the ith neuron of the Mth cluster is as follows.

$$V_{Mi} = \begin{cases} 1, & U_{mi} = max(U_{m1}, \ldots, U_{MN}) \\ 0, & others \end{cases} \quad (1)$$

If there is one or more neurons with the highest input sum in the cluster, the neuron with the index N outputs 1.

B. Switch box routing algorithm using neural network model

The switchbox routing problem can be expressed as an optimization problem to have the minimum number of vias in the switchbox where the existing connection line exists as an obstacle in the internal area. If there are M connection lines and N wiring layers, each neuron has the following energy value.

$$E = \frac{C}{2} \sum_{x=1}^{M} \sum_{y \neq x}^{M} \sum_{i=1}^{N} W_{x,y} V_{x,i} V_{y,i} \quad (2)$$

If the set of Vx,i and Vy,i that minimizes Equation (2) is obtained, it becomes the optimal solution to be obtained, that is, the topological arrangement of each connection line. Wx,y indicates whether the connecting lines intersect each other. If they intersect, it is 1, and if not, it is 0. If Va,i = 1, it indicates that the a-th connection line indicated by Va is in the layer indicated by i.

$$\sum_{i=1}^{N} V_{x,i} = 1, \quad V_{x,i} \in \{1,0 \quad (3)$$

Equation (3) means that each connection line must be located on one of the available layers.

The state equation of the xi-th neuron is:

$$\frac{dU_{x,i}}{dt} = -\frac{\partial E}{\partial V_{x,i}} = -C \sum_{y \neq x}^{N} W_{x,y} V_{y,i} \quad (4)$$

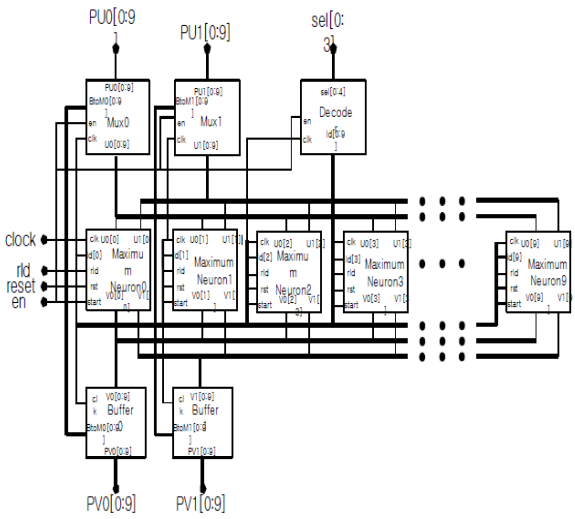


Figure. 1: Block diagram inside switchbox router

When the algorithm proposed in this paper is implemented in hardware, it is necessary to limit the number of wiring layers and connection lines. In this design, a switch box router with 2 wiring layers and 10 connection lines was implemented with ASIC. The structure consists of 10 maximum neurons, Mux, Decoder and Buffer as shown in Figure 2 [7-8,10].

The maximum neuron has input ports U0, U1, clk, rst, ld, rld, and start, and output ports V0 and V1. The PU0 and PU1 ports are used as a common bus by the internal neural network cells, and the initial values and connection matrix information of the neural network cells are input, and the initial values and connectionmatrix information is input to a specific cell among the internal neural network cells according to the values of rld and sel.

If the start signal is enabled after the input, the neural network cell arranges the input line on each wiring layer according to the input of U0 and U1 for each clock with the input information. In this design, all parts could not be implemented as a chip due to size problems, and only one neuron was fully custom-made. The Mux, Decoder, and Buffer implemented the switchbox router hardware at the board level along with the Neural Chip made by implementing the FPGA with Xilnx Viavado's FSKⅢ Device.

IV. CAD TOOL AND FLOW FOR DESIGN

The overall design flow is shown in Figure 3. Sufficient simulations were conducted during the design process, and interfaces between other tools were sufficiently used for design.

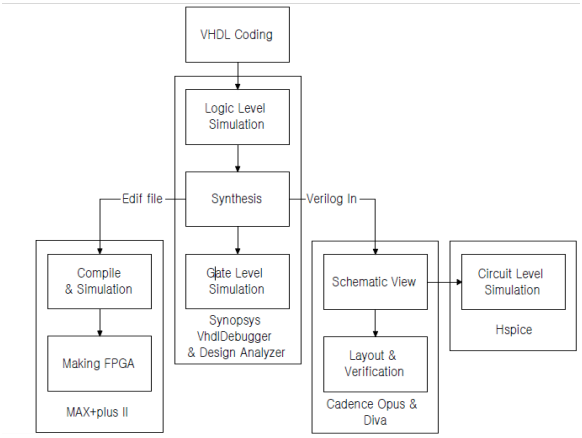


Figure 3: Design Flow

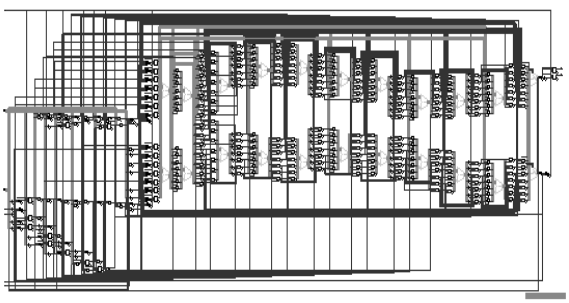


Figure 4: Synopsys Synthesis Schematic

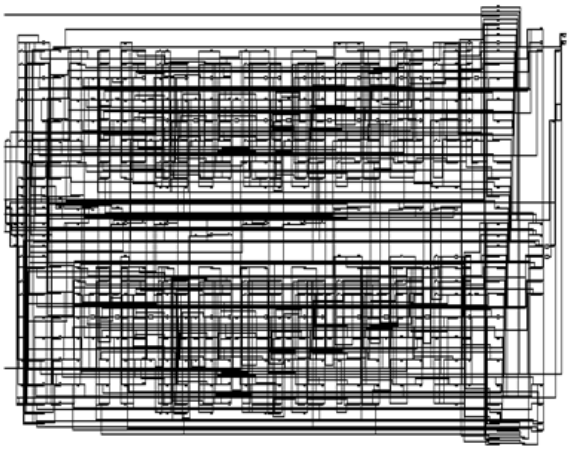


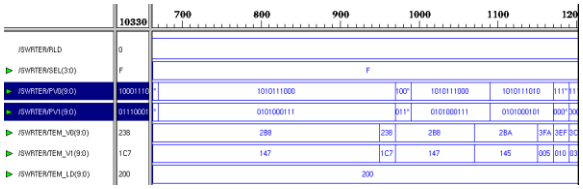
Figure 5: Cadence Schematic

V. HARDWARE DESIGN & SIMULATION

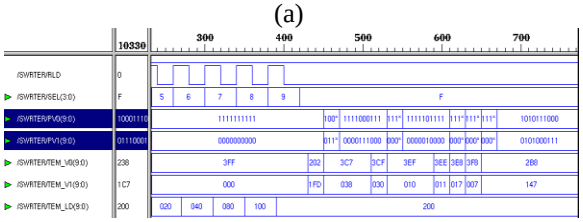
A. Hardware Design

The maximum neuron circuit synthesized with Synopsys' Design Analyzer is shown in Figure 4. After gate simulation of the synthesized circuit, a Schematic View Figure 5 was created using Cadence's Verilog.

B. Simulation

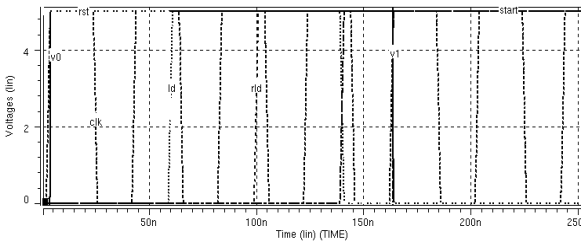


(a)

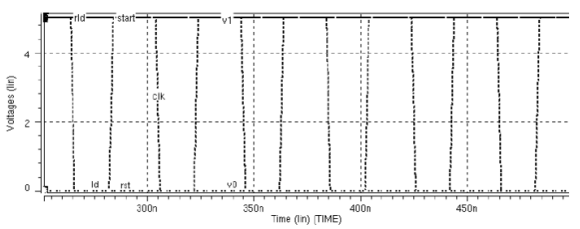


(b)

Figure 6: Logic Level Simulation



(a)



(b)

Figure 7: Circuit Level Simulation

Logic Level Simulation results of the entire switch box router are shown in Figure 6 (a), (b).

The Circuit Level Simulation of the chip fabricated is shown in Figure 7 (a), (b).

C. Layout

As a layout tool, Cadence's Opus tool was used. Figure 8 is the overall layout.

D. Chip Test

The fabricated chip was verified for operation at 3.3V and 5V. For the operation test, the control board implemented with 80196 gave input and monitored the output, and the waveform was output as shown in Figure 9 with HP's 54620A Logic Analyzer.

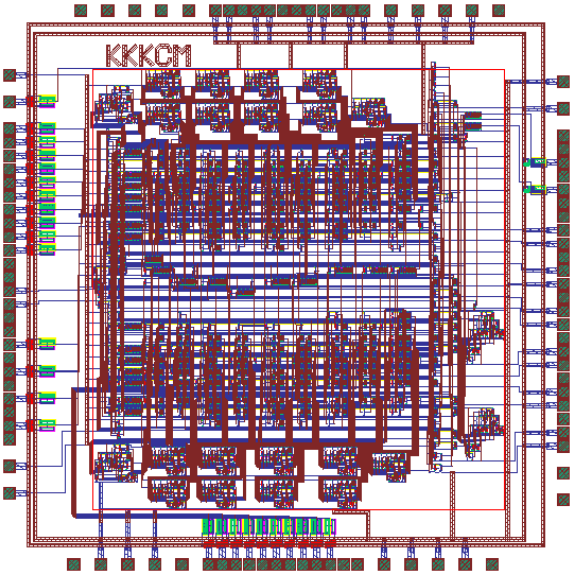


Figure 8: Overall Layout

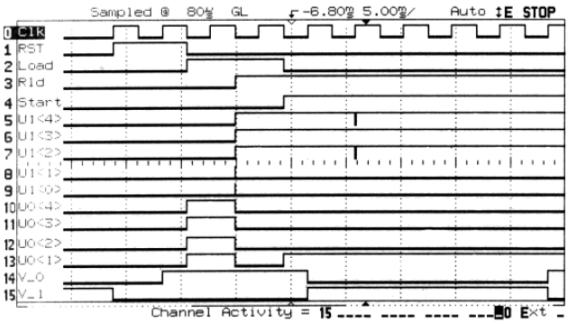


Figure 9: Circuit Level Simulation

As described above, the external blocks Mux, Decoder, and Buffer were implemented with Xilnx Viavado's FSKⅢ Device as FPGA to complete the entire switchbox router. As a result of inputting the connection line information, the problem was solved in about 10-20 Iterations.

VI. CONCLUSION

The switchbox router implemented in this paper is a good example of problem solving using neural networks. Since the neural network is modeled after

the structure of the human brain, it has a structure interconnected with each other, and each neuron independently performs parallel processing. Due to this advantage, it is widely used in pattern recognition.

In the case of the switch box router implemented in this paper, it is possible to allocate 2 wiring layers and 10 connection lines. As in the test results described above, the minimum connection lines are allocated so that the number of vias is about 10-20 times. If the neural network structure is not used and the connection layer is allocated after considering all cases, 210 calculations are required. If the problem is extended to 4 wiring layers and 20 connection lines, 420 operations will be required. However, if implemented with the algorithm of this paper, it is only necessary to expand the state value of neurons from 4 to 2 and only the number of neurons to 20. As a result of the software simulation, about 60-70 calculations were required.

The algorithm proposed in this paper varied the number of wiring layers and connection lines, and as a result of comparing the results with the algorithms of Funabiki and Nichikawa [9], superiority was found.

REFERENCES

[1] M. Sarrafzadeh and D. T. Lee, “A new approach to topological via minimization,” IEEE Trans. Computer-Aided Design, vol.8, pp. 890-900, Aug.1989.

[2] J. J. Hopfield and D. W. Tank, “Neural Computation of Decisions in optimization problems,” Biological Cybernetics, vol. 52, pp. 141-152, 1985.

[3] J. T. Yan and P. Y. Hsiao, "Minimizing the Number of SwitchBox for Region Definition and Ordering Assignment," IEEE Trans. Computer-Aided Design, vol. 15, pp. 336-347, Mar. 1996.

[4] J. Cohoon and P. Heck, "Beaver: A computational-geometry-based tool for switchbox routing," IEEE Trans. Computer-Aided Design, vol. 8, June 1988.

[5] N. Funabiki and Y. Takefuji, "A neural network approach to topological via minimization problems," IEEE Trans. Computer- Aided Design, vol. 12, pp. 770-779, June 1993.

[6] J. J. Hopfield, "Neural networks and physical systems with emergent collective computational abilitues", Proceedings of National Academic Science, Vol. 79, pp. 2554-2588, Biophysics, April 1982.

[7] Y. Takefuji and K. C. Lee, "An Artificial hysteresis binary neural: A model suppressing the oscillatory behaviors of neural dynamics", Biol. Cybern, vol. 64, pp. 353-356, 1991.

[8] M. Marek-Sadowska, "An unconstrained topological via minimization problem for two-layer routing," IEEE Trans. Computer-Aided Design, vol. Cad-3, pp. 184-190, July 1984.

[9] N. Funabiki and S. Nishikawa, "A Neural Network Model for Multilayer Topological Via Minimization in a Switchbox," IEEE Trans. Computer-Aided Design, vol. 15, pp. 1012-1020, August 1996.

[10] Y. B. Cho, "Silicon Neural Networks for Optimization Problems", Case Western Reserve University, May 1992.

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